

**Notice of Allowability**

Application No.

09/991,198

Applicant(s)

HARRISON, RONNIE M.

Examiner

Dung X Nguyen

Art Unit

2631

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--**

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to amendment filed on 07 September 2004.
2. ☒ The allowed claim(s) is/are 17 - 22, renumbered as 1- 6, respectively.
3. ☒ The drawings filed on 07 September 2004 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) ☐ All    b) ☐ Some\*    c) ☐ None    of the:
    1. ☐ Certified copies of the priority documents have been received.
    2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
  6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
    - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
    - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08),  
Paper No./Mail Date \_\_\_\_\_
4. ☐ Examiner's Comment Regarding Requirement for Deposit  
of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413),  
Paper No./Mail Date \_\_\_\_\_
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other \_\_\_\_\_

***EXAMINER'S AMENDMENT***

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Kimton N. Eng, the attorney's applicant, on October 22, 2004.

*IN THE FIGURES (filed on September 07, 2004):*

- In figure 8, on the left corner, at the end of the box 446, a legend of "CLOCK GENERATOR CIRCUIT" within a small box and marked as 447 have been inserted.

*IN THE AMENDMENTS OF SPECIFICATION (filed on September 07, 2004):*

- On page 2, "are" recited on line 8 has been changed to "is". Also, on line 17, after "sequence 460.", "The command buffer 446 includes a clock generator circuit 447 according to embodiment of the present invention to generate the clock signal for synchronizing the received command packets from the command bus 450." has been inserted.

*IN THE CLAIMS:*

- In claim 17, "first" first recited on line 25 has been changed to "the first", "signal" recited on line 25 has been changed to "signals", "the" recited on line 52 has been changed to "a", and "couple" recited on line 84 has been changed to "to couple".

*Allowable Subject Matter*

2. **Claims 17 – 22 are allowed, renumbered as 1 – 6, respectively.** The following is an examiner's statement of reasons for allowance:

Regarding to the claimed invention, the prior art of record fails to show or render obvious of a packetized dynamic random access memory, comprising:

At least one array of memory cells to store data in responsive to a command word;

A row address to receive and decode the row address, and select a row of memory cells corresponding to the row address responsive to the command word;

A column address to receive or apply data to one of memory cells in the selected row corresponding to the column address responsive to the command word;

A data path circuit to couple data between an external terminal and the column address circuit responsive to the command word; and

A command data latch circuit for storing a command data packet at a time determined from a command clock signal, comprising:

- A first delay-locked loop having a first voltage controlled delay circuit receiving a reference clock signal and generating a sequence of clock signals increasing delayed from the reference clock signal to a last clock signal by delaying the reference clock signal by respective delays that are a function of a first control signal, and a first phase detector comparing the phase of a first and second clock signals in the sequence and generating the first control signal as a function of the phase difference therebetween, comprising:
  - A first phase detector circuit having first and second input terminals coupled to receive the first and second clock signals, respectively, and an output terminal, the first phase detector producing a first select signal having duty cycle according to the phase relationship between a first edge and second edge of the first and second clock signals in the sequence;
  - A second phase detector circuit having first and second input terminals coupled to receive the first and second clock signals, respectively, and an

- output terminal, the second phase detector producing a second select signal having duty cycle according to the phase relationship between a first edge and second edge of the first and second clock signals in the sequence;
- A first charge pump having first and second input terminals coupled to the output terminals of the first and second phase detector circuits and an output terminal, the first charge pump producing a non-varying control signal responsive to a first combination of logic levels of the first and second select signals, and increasing control signal responsive to a second combination of logic levels of the first and second select signals, and a decreasing control signal responsive to a third combination of logic levels of the first and second select signals; and
  - A capacitor coupled to the output of the first charge pump;
- A second delay-locked loop having a second voltage controlled delay circuit receiving a master clock signal and generating a reference clock signal having delay relative to the master clock signal that is a function of a second control signal, and a second phase detector comparing the phase of a select one of the clock signals in the sequence and generating the second control signal as a function of the phase difference therebetween, comprising:
- A third phase detector circuit having first and second input terminals coupled to receive the master clock signal and the selected one of the clock signal in the sequence, respectively, and an output terminal, the third phase detector producing a first select signal having duty cycle according to the phase relationship between a first edge and second edge of the master clock signal and the selected one of the clock signals in the sequence;
  - A fourth phase detector circuit having first and second input terminals coupled to receive the master clock signal and the selected one of the clock signals in the sequence, respectively, and an output terminal, the fourth phase detector producing a second select signal having duty cycle according to the phase

relationship between a second edge and second edge of the master clock signal and the selected one of the clock signals in the sequence;

- A second charge pump having first and second input terminals coupled to the output terminals of the third and fourth phase detector circuits, the second charge pump producing a non-varying control signal responsive to a first combination of logic levels of the first and second select signals, and increasing control signal responsive to a second combination of logic levels of the first and second select signals, and a decreasing control signal responsive to a third combination of logic levels of the first and second select signals; and
- A capacitor coupled to the output of the second charge pump;
- A multiplexer coupled to the first delay-lock loop to receive the clock signals in the sequence and coupled one of the clock signals in the sequence to the clock input of the latch circuit, the clock signal coupled to the latch circuit being selected by the multiplexer as a function of a select signal applied to a control input of the multiplexer; and
- A select circuit determining which of the clock signals from the first delay-lock loop should be used to cause the latch circuit to store the command data packet and generating the select signal corresponding thereto.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

### ***Contact Information***

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung X. Nguyen whose telephone number is (571) 272-3010. The examiner can normally be reached on Monday through Friday from 8:00 AM to 17:00 PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Ghayour Mohammad H. can be reached on (571) 272-3021. The fax phone numbers for this group is (571) 273-3021.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2600.

DXN

October 24, 2004

M. Gh-  
MOHAMMED GHAYOUR  
SUPERVISORY PATENT EXAMINER